ISO 9001 Registered

IMP5115
9-Line SCSI Terminator
–DS21S07A Upgrade

DESCRIPTION

The IMP5115 SCSI terminator is part of IMP's family of high-performance, adaptive, non-linear mode SCSI products, which are designed to deliver true UltraSCSI performance in SCSI applications. The low voltage BiCMOS architecture employed in its design offers performance superior to older linear passive and active techniques. IMP's SCSI termination architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible — typically 35MHz, which is 100 times faster than the older linear regulator/ terminator approach used by other manufacturers. Products using this older linear regulator approach have bandwidths which are dominated by the output capacitor and which are limited to 500KHz (see further discussion in the Functional Description section). This new architecture also eliminates the output compensation capacitor required in earlier terminator designs. Each is approved for use with SCSI-1, -2, -3, UltraSCSI and beyond — providing the highest performance alternative available today.

Another key improvement offered by the IMP5115 lies in its ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as the use of improper cable lengths and impedances. Frequently, this situation is not controlled by the peripheral or host designer and, when problems occur, they are the first to be made aware of the problem. The IMP5115 architecture is much more tolerant of marginal system integrations.

Recognizing the needs of portable and configurable peripherals, the IMP5115 has a TTL compatible sleep/disable mode. Quiescent current is typically less than 375µA in this mode, while the output capacitance is also less than 3pF. The obvious advantage of extended battery life for portable systems is inherent in the product's sleep-mode feature. Additionally, the disable function permits factory-floor or production-line configurability, reducing inventory and product-line diversity costs. Field configurability can also be accomplished without physically removing components which, often times results in field returns due to mishandling.

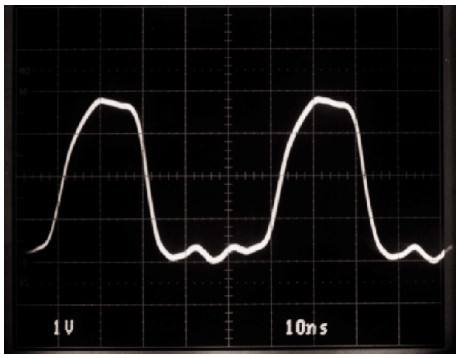
Reduced component count is also inherent in the IMP5115 architecture. Traditional termination techniques require large stabilization and transient protection capacitors of up to 20µF in value and size. The IMP5115 architecture does not require these components, allowing all the cost savings associated with inventory, board space, assembly, reliability, and component costs.

KEY FEATURES

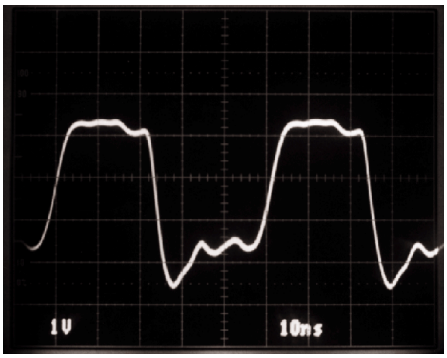
- ULTRA-FAST RESPONSE FOR FAST-20 SCSI APPLICATIONS
- 35MHz CHANNEL BANDWIDTH
- 3.5V OPERATION
- LESS THAN 3pF OUTPUT CAPACITANCE
- SLEEP-MODE CURRENT LESS THAN 375µA
- THERMALLY SELF LIMITING
- NO EXTERNAL COMPENSATION CAPACITORS
- IMPLEMENTS 8-BIT OR 16-BIT (*WIDE*) APPLICATIONS
- COMPATIBLE WITH ACTIVE NEGATION DRIVERS (60mA / CHANNEL)
- COMPATIBLE WITH PASSIVE AND ACTIVE TERMINATIONS
- APPROVED FOR USE WITH SCSI 1, 2, 3 AND ULTRA SCSI
- HOT SWAP COMPATIBLE
- PIN-FOR-PIN COMPATIBLE WITH DS21S07A / 2105

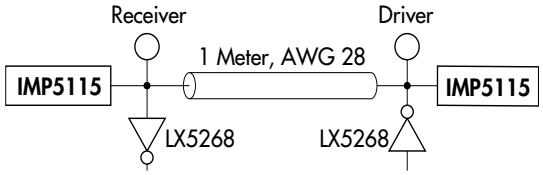
PRODUCT HIGHLIGHT

RECEIVING WAVEFORM - 20MHz



DRIVING WAVEFORM - 20MHz





PACKAGE ORDER INFORMATION

T_J(°C)	D Plastic SOIC 16-pin	DW Plastic SOWB 16-pin	PWP Plastic TSSOP 20-pin, Power
0 to 125	IMP5115CD	IMP5115CDW	IMP5115CPWP

Note: All surface-mount packages are available in Tape & Reel.
Append the letter "T" to part number. (i.e. IMP5115CDWT)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Continuous Termination Voltage 10V
Continuous Output Voltage Range ..... 0 to 5.5V
Continuous Disable Voltage Range ..... 0 to 5.5V
Operating Junction Temperature ..... 0°C to 125°C
Storage Temperature Range ..... -65°C to +150°C
Solder Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DATA

D PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, Q_{JA} ..... 120°C/W

DW PACKAGE:

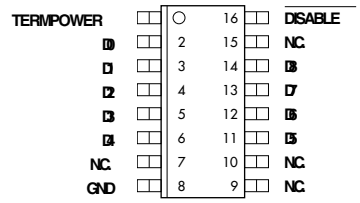
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Q_{JA} ..... 95°C/W

PWP PACKAGE:

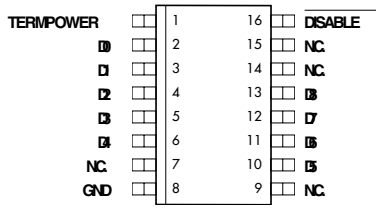
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Q_{JA} ..... 139°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no ambient airflow.

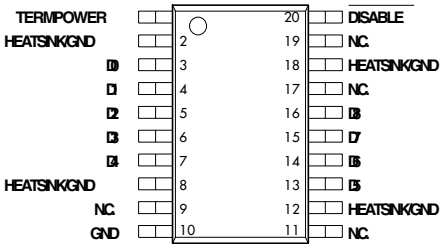
PACKAGE PIN OUTS



D PACKAGE
(Top View)



DW PACKAGE
(Top View)



PWP PACKAGE
(Top View)

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Termination Voltage	V_{TERM}	3.5		5.5	V
High Level Enable Input Voltage	V_{IH}	2		V_{TERM}	V
Low Level Disable Input Voltage	V_{IL}	0		0.8	V
Operating Virtual Junction Temperature Range					
IMP5115C		0		125	°C

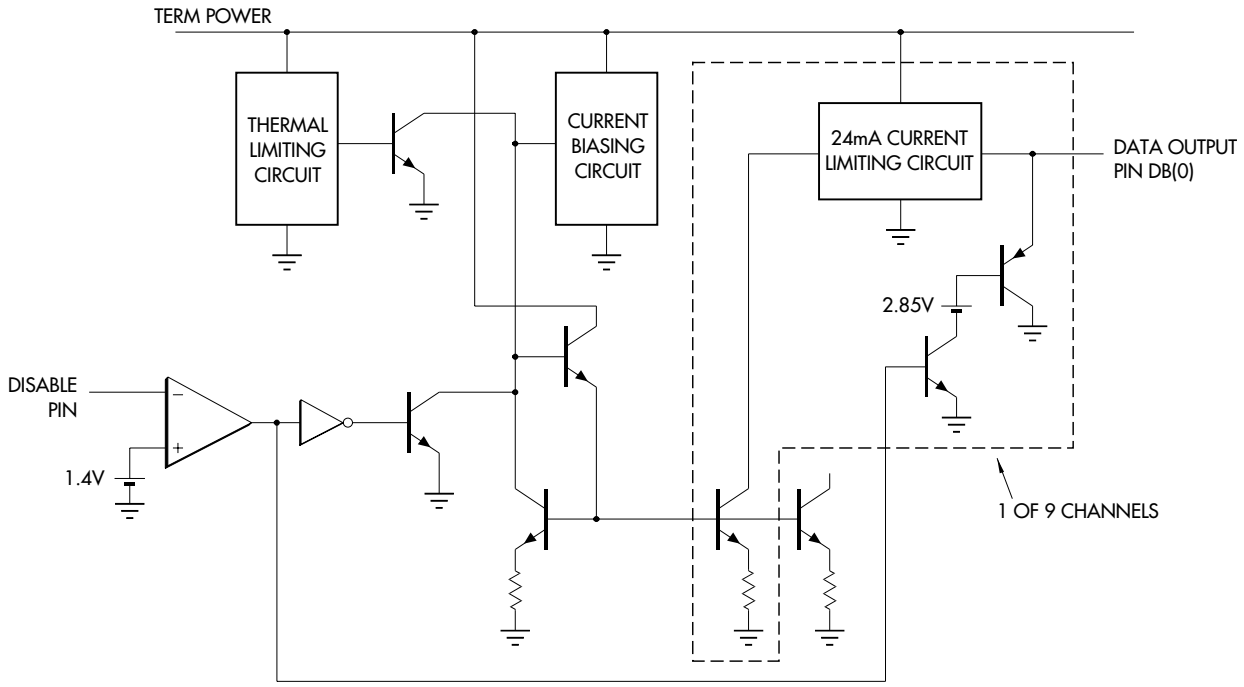
Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

Term Power = 4.75V unless otherwise specified. Unless otherwise specified, these specifications apply at the recommended operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Test Conditions	IMP5115			Units
			Min.	Typ.	Max.	
Output High Voltage	V_{OUT}		2.65	2.85		V
TermPwr Supply Current	I_{CC}	All data lines = open		6	9	mA
		All data lines = 0.5V		215	225	mA
		Disable Pin < 0.8V		375		µA
Output Current	I_{OUT}	V_{OUT} = 0.5V	-21	-23	-24	mA
Disable Input Current	I_{IN}	Disable Pin = 4.75V		10		nA
		Disable Pin = 0V		-90		µA
Output Leakage Current	I_{OL}	Disable Pin = < 0.8V, V_O = 0.5V		10		nA
Capacitance in Disabled Mode	C_{OUT}	V_{OUT} = 0V, frequency = 1MHz		3		pF
Channel Bandwidth	BW			35		MHz
Termination Sink Current, per Channel	I_{SINK}	V_{OUT} = 4V		60		mA

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators, which consist of Linear Regulators in series with resistors (typically 110Ω), are a compromise. As the line voltage increases, the amount of current decreases linearly by the equation V = I * R. The IMP5115, with its unique new architecture applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Acting as a near ideal line terminator, the IMP5115 closely reproduces the optimum case when the device is enabled. To enable the device the Disable Pin must be pulled Logic High or left open. During this mode of operation, quiescent current is 6mA and the device will respond to line demands by delivering 24mA on assertion and by imposing 2.85V on deassertion. In order to disable the device, the Disable pin must be driven logic **Low**. This mode of operation places the device in a sleep state where a meager 375µA of quiescent current is consumed. Additionally, all outputs are in a Hi-Z (impedance) state. Sleep mode can be used for power conservation or to completely eliminate the terminator from the SCSI chain. In the second case, termination node capacitance is important to consider. The terminator will appear as a parasitic distributed capacitance on the line, which can detract from bus performance. For this reason, the IMP5115 has been optimized to have only 3pF of capacitance per output in the sleep state.

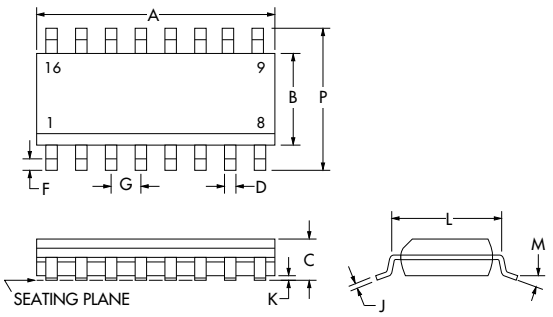
An additional feature of the IMP5115 is its compatibility with active negation drivers. The device handles up to 60mA of sink current for drivers which exceed the 2.85V output high.

POWER UP / POWER DOWN FUNCTION TABLE

Disable IMP5115	Outputs	Quiescent Current
H	Enabled	6mA
L	HI Z	375µA
Open	Enabled	6mA

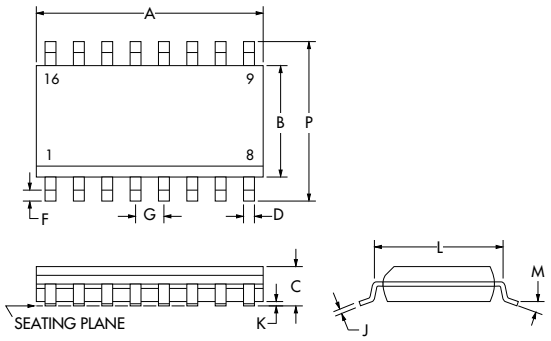
PACKAGE DIMENSIONS

D 16-Pin Plastic S.O.I.C.



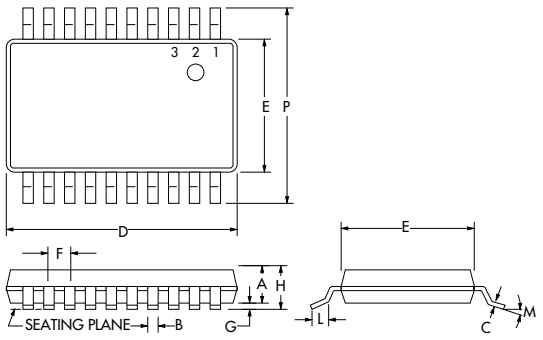
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.51	0.77	0.020	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.007	0.010
K	0.10	0.25	0.004	0.010
L	4.82	5.21	0.189	0.205
M	0°	8°	0°	8°
P	5.79	6.20	0.228	0.244

DW 16-Pin Plastic (SOWB) Widebody S.O.I.C.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	10.67	—	0.420
B	7.49	7.75	0.295	0.305
C	2.35	2.65	0.093	0.104
D	0.25	0.46	0.010	0.018
F	0.64	0.89	0.025	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.10	0.30	0.004	0.012
L	8.13	8.64	0.320	0.340
M	0°	8°	0°	8°
P	10.26	10.65	0.404	0.419

PWP 20-Pin Thin Small Shrink Outline (TSSOP)



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	0.90	—	0.354
B	0.18	0.30	0.0071	0.0118
C	0.90	0.180	0.0035	0.0071
D	6.40	6.60	0.252	0.260
E	4.30	4.48	0.169	0.176
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	—	1.10	—	0.0433
L	0.50	0.70	0.020	0.028
M	0°	8°	0°	8°
P	6.25	6.50	0.246	0.256

ISO 9001 Registered

IMP, Inc.
Corporate Headquarters
2830 N. First Street
San Jose, CA 95134
Tel: 408.432.9100 Main
Tel: 800.438.3722
Fax: 408.434.0335
e-mail: info@impinc.com
http://www.impweb.com

The IMP logo is a registered trademark of IMP, Inc.
All other company and product names are trademarks of their respective owners.

© 1999 IMP, Inc.
Printed in USA

Publication #: 7006
Revision: A
Issue Date: 09/09/97
Type: Product